In the Specification:

Please amend the first paragraph on page 1 as follows:

This application is a continuation-in-part of co-pending U.S. Patent Application Serial No. 10/765,802 filed January 26, 2004 entitled "HIGH DENSITY SEMICONDUCTOR MEMORY CELL AND MEMORY ARRAY USING A SINGLE TRANSISTOR AND HAVING VARIABLE GATE OXIDE BREAKDOWN", which is a continuation-in-part of co-pending U.S. Patent Application Serial No. 10/677,613 filed October ~~1~~2, 2003 entitled "HIGH DENSITY SEMICONDUCTOR MEMORY CELL AND MEMORY ARRAY USING A SINGLE TRANSISTOR HAVING A BURIED N+ CONNECTION", which is a continuation-in-part of co-pending U.S. Patent Application Serial No. 10/448,505 filed May 30, 2003 entitled "HIGH DENSITY SEMICONDUCTOR MEMORY CELL AND MEMORY ARRAY USING A SINGLE TRANSISTOR" and co-pending U.S. Patent Application Serial No. 10/133,704 filed April 26, 2002 entitled "HIGH DENSITY SEMICONDUCTOR MEMORY CELL AND MEMORY ARRAY USING A SINGLE TRANSISTOR", to which priority from all is hereby claimed under 35 USC § 120.